REMARKS

Claims 1-13 are pending. Claim 6 has been canceled. The drawing have been amended as required by the Examiner. The specification has been amended to include the serial number of the co-pending application, and other informalities listed by the Examiner. No new matter has been entered by way of this amendment. Reconsideration of the application is requested.

The Examiner has objected to claims 1, 4-7, 11 and 12. Applicant submits that the objections to the claims have been addressed by the amendments herein, with a view to each rejection raised in the Office Action. Accordingly, reconsideration and withdrawal of the objections are respectfully requested.

The drawing have been objected to. Specifically, the Examiner has objected to Fig. 6 and Fig. 7. Concurrently, herewith Applicant has submitted a request to Request to Change Drawings that addresses each and ever objection raised by the Examiner. Accordingly, reconsideration and withdrawal of the objections are respectfully requested.

Claim 11 stands rejected under 35 U.S.C. §102(e) as being rejected by U.S. Patent No. 5,996,006 to *Yung*, while claims 1, 2-10, 12, and 13 have been rejected as being unpatentable over the same reference in view of *Michael J. Flynn*, "Computer Architecture; Pipelined and Parallel Processor Design. 1995." (hereafter *Flynn*) These rejections are respectfully traversed.

Independent claims 1 and 8 have been amended to include the elements "each input store holds a plurality of objects of a predetermined size, each object defining one of a plurality of lanes, a maximum number of lanes being determined by the smallest predetermined object size" and "the number of said stored condition values corresponds to said maximum number of lanes in each of said first and second input stores, a prior operation being operable to

generate said condition values so that, when the operands have less than the maximum number of lanes, two or more condition values are set to the same value so that each individual condition value is generated regardless of the degree of packing of the first and second source operands." Support for this limitation may be found, for example, on page 4 of the specification, thus this limitation does not constitute new matter.

Yung et al. is directed to an optimized, superscalar microprocessor architecture for supporting graphics operations in addition to the standard microprocessor integer and floating point operations. According to this patent, a number of specialized graphics instructions and accompanying hardware for executing them are disclosed to optimize the execution of graphics instruction with minimal additional hardware for a general purpose CPU. However, this reference fails to teach the limitation as set forth in amended independent claims 1 and 8. In addition, this reference fails to teach a system supporting input objects of varying predetermined sizes and having the claimed capabilities of the present invention.

Flynn fails to cure the deficiencies of the *Yung* patent. The *Flynn* reference is mainly relied upon to teach Condition Code Testing (see page 9, paragraph 19 of the Office Action). Specifically, *Flynn* fails to teach the elements "each input store holds a plurality of objects of a predetermined size, each object defining one of a plurality of lanes, a maximum number of lanes being determined by the smallest predetermined object size" and "the number of said stored condition values corresponds to said maximum number of lanes in each of said first and second input stores, a prior operation being operable to generate said condition values so that, when the operands have less than the maximum number of lanes, two or more condition values are set to the same value so that each individual condition value is generated regardless of the degree of packing of the first and second source operands." Further, *Flynn* also fails to teach

a system supporting input objects of varying predetermined sizes and having the claimed capabilities of the present invention. Hence this reference does not cure the deficiency of the Yung patent.

In sum, none of the cited reference teaches or suggests, either individually or in combination, an execution unit capable; of conditionally executing instructions on objects of varying predetermined sizes and having condition values capable of being set individually or in pluralities as claimed. This feature permits the use of a common instruction format in condition value setting and data processing operations. Accordingly Applicant submits that amended independent claims 1 and 8 are patentable over the cited prior art.

In view of the patentability of independent claims 1 and 8, for the reasons above, dependent claims 2-5 and 9-13 are patentable over the prior art.

In view of the foregoing remarks, the application is respectfully submitted to be in condition for allowance and prompt, favorable action thereon is earnestly solicited. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested. However, should the Examiner believe that direct contact with Applicant's attorney would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

Respectfully submitted,

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